UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,516	11/26/2001	Trung T. Doan	500966.01	8536

7590 12/23/2005

Kimton N. Eng, Esq.
DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101

EXAMINER	
CLEARY, THOMAS J	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,516	DOAN ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,11-16,18-22,25-27,33,34,36-42,44-48 and 50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,11-16,18-22,25-27,33,34,36-42,44-48 and 50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, 15, 16, 19, 20, 21, 22, 25, 26, 27, 33, 34, 36, 37, 38, 39, 40, 41, 42, 44, 45, 46, 47, 48, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,256,692 Yoda et al. ("Yoda"), US Patent Number 6,098,158 to Lay et al. ("Lay"), and US Patent Number 5,818,182 to Viswanadham et al. ("Viswanadham").

3. In reference to Claim 1, Yoda teaches a central processing unit (CPU) (See Figure 1 Number 10); a local CPU bus coupled to the CPU (See Figure 1 Number 14); a memory coupled to the local CPU bus to store data accessible by the CPU via the local CPU bus (See Figure 1 Number 12); a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus (See Figure 1 Number 18); and a PC card coupled to the PCI bus (See Figure 1 Number 26), the PC card further having a controller coupled to the PC card device for coordinating with the

CPU access to the device (See Figure 1 Number 28); and a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC Card coupled to the PCI-CardBus bridge (See Figure 1 Number 24). Yoda does not teach the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 6 Lines 36-43). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not

require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

4. In reference to Claim 4, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 1 above. Viswanadham further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Column 1 Lines 59-61).

5. In reference to Claim 5, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 1 above. Yoda further teaches that the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the PC card device and the controller to transfer data between the device and the PCI bus in accordance with a data format and transfer protocol of the PCI bus (See Figure 1 Number 27). The PCMCIA card inherently includes a controller for transferring data between the flash memory and the attached bus in accordance with the data format and transfer protocol of the attached bus.

6. In reference to Claim 6, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 1 above. Lay further teaches a transfer component directing the controller to coordinate access between the non-volatile memory and the memory to transfer machine state information (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

7. In reference to Claim 7, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 1 above. Yoda, Lay, and Viswanadham do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

8. In reference to Claim 8, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 1 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

9. In reference to Claim 9, Yoda teaches a central processing unit (CPU) (See Figure 1 Number 10); a memory coupled to the CPU to store data accessible by the CPU (See Figure 1 Number 12); a bus coupled to the CPU and the memory to provide communication therewith (See Figure 1 Number 18); and a PC card coupled to the bus

(See Figure 1 Number 26), the PC card further having a controller coupled to the PC card device for coordinating with the CPU access to the device (See Figure 1 Number 28), wherein the bus comprises a PCI bus (See Figure 1 Number 18), and the computer system further comprises a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC card coupled to the PCI-CardBus bridge (See Figure 1 Number 24). Yoda does not teach the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory for coordinating with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to

boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

10. In reference to Claim 11, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 9 above. Viswanadham further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Column 1 Lines 59-61).

11. In reference to Claim 12, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 9 above. Yoda further teaches that the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the PC card device and the controller to transfer data between the device and the PCI bus in accordance with a data format and transfer protocol of the PCI bus (See Figure 1 Number 27). The PCMCIA card inherently includes a controller for transferring data between the flash memory and the attached bus in accordance with the data format and transfer protocol of the attached bus.

12. In reference to Claim 13, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 9 above. Lay further teaches a transfer component directing the

controller to coordinate access between the non-volatile memory and the memory to transfer machine state information (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63).

13. In reference to Claim 14, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 9 above. Yoda, Lay, and Viswanadham do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

14. In reference to Claim 15, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 9 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

15. In reference to Claim 16, Yoda teaches an apparatus having a central processing unit (CPU) (See Figure 1 Number 10) coupled to a memory (See Figure 1 Number 12) via a first bus (See Figure 1 Number 14), and further having a PCI bus coupled to the first bus to provide communication with the CPU and the memory (See Figure 1 Number 18); and a PC card coupled to the PCI bus (See Figure 1 Number 26), the PC card further having a controller coupled to the PC card device for coordinating with the CPU access to the device (See Figure 1 Number 28); and a bus interface compatible with a CardBus and coupled to the PCI bus, the bus interface further coupled to the PC card device and the controller to transfer data between the device and the PCI bus in accordance with a data format and transfer protocol of the PCI bus (See Figure 1 Number 27). Yoda does not teach that the apparatus is for capturing and restoring a machine state of a computer system, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer

component directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

16. In reference to Claim 19, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 16 above. Viswanadham further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Column 1 Lines 59-61).

17. In reference to Claim 20, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 16 above. Lay further teaches the transfer component comprises: a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory (See Figure 3, Column 2 Lines 26-31, and Column 2 Lines 45-54); and a download component for directing the controller to transfer data from the nonvolatile memory to the CPU and the memory (See Figure 5, Column 3 Lines 2-5, and Column 5 Lines 32-63).

18. In reference to Claim 21, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 16 above. Yoda, Lay, and Viswanadham do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

19. In reference to Claim 22, Yoda teaches an apparatus having a central processing unit (CPU) (See Figure 1 Number 10) coupled to a memory (See Figure 1 Number 12), and further having a PCI bus coupled to the CPU and memory to provide

communication with the CPU and the memory (See Figure 1 Number 18); and a PC card coupled to the PCI bus (See Figure 1 Number 26), the PC card further having a controller coupled to the PC card device for coordinating with the CPU access to the device (See Figure 1 Number 28); and a CardBus compatible bus interface coupled to the PCI bus, and further coupled to the PC card device and the controller to transfer data between the device and the PCI bus in accordance with a data format and transfer protocol of the PCI bus (See Figure 1 Number 27). Yoda does not teach that the apparatus is for capturing and restoring a machine state of a computer system, the PC card having a non-volatile memory for storing machine state information corresponding to the machine state, and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, and Column 3 Lines 2-5); and a transfer component directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54,

Column 3 Lines 2-5, and Column 5 Lines 39-63). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

20. In reference to Claim 25, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 23 above. Viswanadham further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Column 1 Lines 59-61).

21. In reference to Claim 26, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 23 above. Lay further teaches the transfer component comprises: a storing component for directing the controller to store machine state information from the CPU and memory to the non-volatile memory (See Figure 3, Column 2 Lines 26-31, and Column 2 Lines 45-54); and a download component for directing the controller to

transfer data from the nonvolatile memory to the CPU and the memory (See Figure 5, Column 3 Lines 2-5, and Column 5 Lines 32-63).

22. In reference to Claim 27, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 23 above. Yoda, Lay, and Viswanadham do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

23. In reference to Claim 33, Yoda teaches a central processing unit (CPU) (See Figure 1 Number 10); a local CPU bus coupled to the CPU (See Figure 1 Number 14); a memory coupled to the local CPU bus to store data accessible by the CPU via the local CPU bus (See Figure 1 Number 12); a PCI bus coupled to the local CPU bus to provide communication with the CPU and the memory via the local CPU bus (See Figure 1 Number 18); a PCI-CardBus bridge coupled to the PCI bus to provide communication between the PCI bus and the PC Card coupled to the PCI-CardBus bridge (See Figure 1 Number 24); a CardBus compatible PC card coupled to the PCI-CardBus bridge (See

Figure 1 Number 26), the PC card further having a controller coupled to the PC card device for coordinating with the CPU access to the device (See Figure 1 Number 28); and wherein the PC card further includes a bus interface coupled to the PCI bus, and further coupled to the PC card device and the controller to transfer data between the device and the PCI bus in accordance with a data format and transfer protocol of the PCI bus (See Figure 1 Number 27). Yoda does not teach the PC card having a non-volatile memory for storing machine state information and further having a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system. Lay teaches storing machine state information in a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5) and a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 6 Lines 36-43); and a transfer component for directing the controller to coordinate with the CPU access to the non-volatile memory and the memory to store and download the machine state information for capturing and restoring, respectively, a corresponding machine state of a computer system (See Figures 4 and 6, Column 2 Lines 26-31, Column 2 Lines 45-54, Column 3 Lines 2-5, and Column 5 Lines 39-63). Viswanadham teaches PCMCIA card, which is compatible

with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

24. In reference to Claim 34, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 33 above. Viswanadham further teaches that the non-volatile memory of the PC card comprises a flash memory device (See Column 1 Lines 59-61).

25. In reference to Claim 36, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 33 above. Yoda, Lay, and Viswanadham do not teach compression and decompression components for compressing the machine state information to be stored and decompressing the stored compressed machine state information to be downloaded, respectively. Lay, however, teaches that it is well known to compress an

image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

26. In reference to Claim 37, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 33 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

27. In reference to Claim 38, Yoda teaches a computer system having a central processing unit (CPU) (See Figure 1 Number 10) coupled to a memory (See Figure 1 Number 12), and further having a bus coupled to the CPU and memory to provide communication therewith (See Figure 1 Number 14), a PC card (See Figure 1 Number 26), and wherein transferring information to the PC card comprises transferring data from the CPU and the memory to the PC card in accordance with a CardBus protocol (See Figure 1 Number 24). Yoda does not teach a method for storing a machine state of the computer system, comprising: capturing the machine state of the computer system via a controller coupled to a non-volatile memory to control the storing of data therein and the retrieval of data therefrom; transferring machine state information

corresponding to the captured machine state from the computer system to a PC card operably coupled with the non-volatile memory; and storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system. Lay teaches capturing the machine state of the computer system via a controller coupled to a non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Column 2 Lines 26-37); transferring machine state information corresponding to the captured machine state from the computer system to a non-volatile memory (See Figure 4 and Column 2 Line 23 – Column 3 Line 5); and storing the machine state information in the non-volatile memory in order to restore the stored machine state when the machine state information is provided to a computer system (See Figure 4 and Column 2 Line 23 – Column 3 Line 5). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not require drive motors (See Column 1 Lines 64-67), can be easily transported between

multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

28. In reference to Claim 39, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 38 above. Lay further teaches that capturing, transferring and storing the machine state information is in response to executing a power down procedure (See Column 4 Lines 20-25).

29. In reference to Claim 40, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 38 above. Lay further teaches that capturing, transferring and storing the machine state information is in response to a user request (See Column 4 Lines 20-25, Column 4 Lines 41-55, and Column 5 Lines 36-38).

30. In reference to Claim 41, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 38 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

31. In reference to Claim 42, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 38 above. Lay further teaches that capturing the machine state of the computer system comprises: capturing data present in the memory (See Column 2

Lines 33-37); and capturing data present in registers of the CPU (See Column 5 Lines 1-6).

32. In reference to Claim 44, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 38 above. Yoda, Lay, and Viswanadham do not teach compressing the machine state information to be stored in the non-volatile memory. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

33. In reference to Claim 45, Yoda teaches a computer system having a central processing unit (CPU) (See Figure 1 Number 10) coupled to a memory (See Figure 1 Number 12), and further having a bus coupled to the CPU and memory to provide communication therewith (See Figure 1 Number 18), and a PC card (See Figure 1 Number 26), and wherein transferring information from the PC card device comprises transferring data from the PC card to the computer system in accordance with a CardBus protocol (See Figure 1 Number 24). Yoda does not teach a method for restoring a machine state of the computer system, comprising: identifying machine state information corresponding to the machine state to which the computer system is to be

restored stored in a non-volatile memory included in a PC card; transferring the machine state information from the non-volatile memory to the computer system via a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom; and writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state. Lay teaches identifying machine state information corresponding to the machine state to which the computer system is to be restored stored in a non-volatile memory (See Column 5 Lines 41-44); transferring the machine state information from the non-volatile memory to the computer system via a controller coupled to the non-volatile memory to control the storing of data therein and the retrieval of data therefrom (See Figure 6 and Column 5 Lines 44-46); and writing data of the machine state information to the memory and CPU in order to restore the computer system to the identified machine state (See Figures 5 and 6 and Column 5 Lines 53-63). Viswanadham teaches PCMCIA card, which is compatible with CardBus and can be used in a CardBus slot, having a non-volatile memory as the card device (See Column 1 Line 59 – Column 2 Line 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the computer system of Yoda with the fast boot by saving the system state to non-volatile memory of Lay in order to allow the system to boot up faster (See Column 1 Lines 39-50 and Column 2 Lines 23-40 of Lay). It would have been further obvious to place the non-volatile memory on the PCMCIA card of Viswanadham because PCMCIA memory cards are small, lightweight, and do not

require drive motors (See Column 1 Lines 64-67), can be easily transported between multiple computer systems, thus allowing the multiple systems to operate on a single set of data, and because PCMCIA was designed for memory cards.

In reference to Claim 46, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 45 above. Lay further teaches that identifying, transferring and writing the machine state information is in response to executing a power up procedure (See Column 4 Lines 20-25 and Column 5 Lines 32-34).

34. In reference to Claim 47, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 45 above. Lay further teaches that identifying, transferring and writing the machine state information is in response to a user request (See Column 4 Lines 20-25, Column 4 Lines 41-55, and Column 5 Lines 36-38).

35. In reference to Claim 48, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 45 above. Lay further teaches that the machine state information comprises data from the memory and CPU for returning the computer system to the same condition of operability as when the machine state information was stored in the non-volatile memory (See Figure 3 and Column 2 Lines 26-37).

36. In reference to Claim 50, Yoda, Lay, and Viswanadham teach the limitations as applied to Claim 45 above. Yoda, Lay, and Viswanadham do not teach that the

machine state information stored in the non-volatile memory is in a compressed data format, and the method further comprises decompressing the machine state information to be transferred to the computer system. Lay, however, teaches that it is well known to compress an image of the machine state information to be saved to disk, and to later decompress the image when booting the system (See Column 1 Lines 51-60).

It would have been obvious to compress the image of the machine state because it is well known that compressed data takes up less space in memory than uncompressed data, thus allowing more efficient use of the memory space.

Claim Rejections - 35 USC § 112

37. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the Applicant regards as his invention.

38. Claims 1, 4, 5, 6, 7, 8, 9, 11, 12, 13, 14, and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

39. Claim 1 recites the limitations of "a PC card coupled to the PCI bus" and "the PC card coupled to the PCI-CardBus bridge. Claim 9 recites the limitations of "a PC card coupled to the bus" and "the PCI card coupled to the PCI-CardBus bridge. It is unclear

how the PC card can be coupled to both the PC card and the PCI-CardBus bridge, as the PCI-Cardbus bridge is located between the PC card and the PCI bus.

Claim Objections

40. Claim 5 is objected to because of the following informalities: Claim 5, which has been amended, has an incorrect status identifier. Appropriate correction is required.

Response to Arguments

41. Applicant's arguments with respect to Claims 1, 4-9, 11-16, 18-22, 25-27, 33-34, 36-42, 44-48, and 50 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

42. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 6,799,247 to Batcher, which teaches that many typical embedded systems use a CardBus interface (See Column 3 Lines 49-51); and US Patent Number 5,902,991 to Kumar, which teaches the use of a PCMCIA memory card.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/19/05

Thomas J. Cleary
Patent Examiner
Art Unit 2111